

Patent Points

NOW STARTING MY 33ND YEAR...

Wet Chemical Patent

Most of the 600+ issued patents I have written are in electronics or software since I worked as a design engineer for 9 years before moving to patent writing. While my master's degree was in Electrical Engineering, my bachelor's degree was in Chemical Engineering.

I recently had the opportunity to write a chemical patent. US Patent #12,529,159 is for "Co-electroplating Sn—Bi alloy solder for 3D-IC low-temperature bonding". Three chemicals are added to an electrolyte bath to co-deposit tin-bismuth alloys. Traditional solder alloys have lead, which is toxic, so replacing lead with Bismuth is desirable. However, getting an alloy with a low melting point is tricky, requiring a specific % composition of the Bismuth.

A more typical electronics patent is shown on page 3. The well-known Harvard Architecture has separate Instruction and Data buses.

However, having separate buses makes debugging difficult as the Instructions in the Instruction memory are hidden from any debugger connected to the Data bus.

The inventors add a special Debug mode to allow the

Instruction bus to be accessed by the Data bus. Thus the debugger can read both Instructions and Data.

Copies of the patents are shown on the next pages.

Congratulations to all the inventors !

Ribbon Copy Phaseout

The US Patent Office for years has issued a special bound patent known as a "Ribbon Copy" due to a ribbon that was attached to an embossed seal on the ceremonial cover. Only a single copy was provided for each patent. If lost, the ribbon copy was difficult or impossible to replace. When patents were sold with missing ribbon copies the buyer would often demand a reduced price.

The USPTO has moved to providing an electronic copy known as the e-grant, which is downloaded from the PTO website as a pdf. The e-grant is now considered to be the official copy while the ribbon copy is ceremonial only and is provided only upon request when paying the issue fee.

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- 2** Chemical Patent
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US012529159B2

(12) **United States Patent**
Xu et al.

(10) **Patent No.:** **US 12,529,159 B2**
(45) **Date of Patent:** **Jan. 20, 2026**

(54) **CO-ELECTROPLATING Sn—Bi ALLOY
SOLDER FOR 3D-IC LOW-TEMPERATURE
BONDING**

(71) Applicant: **Hong Kong Applied Science and
Technology Research Institute
Company Limited**, Hong Kong (HK)

(72) Inventors: **Minjie Xu**, Hong Kong (HK); **Xunqing
Shi**, Hong Kong (HK); **Pau Yee Lim**,
Hong Kong (HK); **Tsz Fung Au**, Hong
Kong (HK)

(73) Assignee: **Hong Kong Applied Science and
Technology Research Institute
Company Limited**, Hong Kong (HK)

(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 28 days.

(21) Appl. No.: **18/390,167**

(22) Filed: **Dec. 20, 2023**

(65) **Prior Publication Data**
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12, 2023.
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C25D 3/60 (2006.01)
C25D 17/14 (2006.01)
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(2013.01); **C25D 17/14** (2013.01)
(58) **Field of Classification Search**
None
See application file for complete search history.

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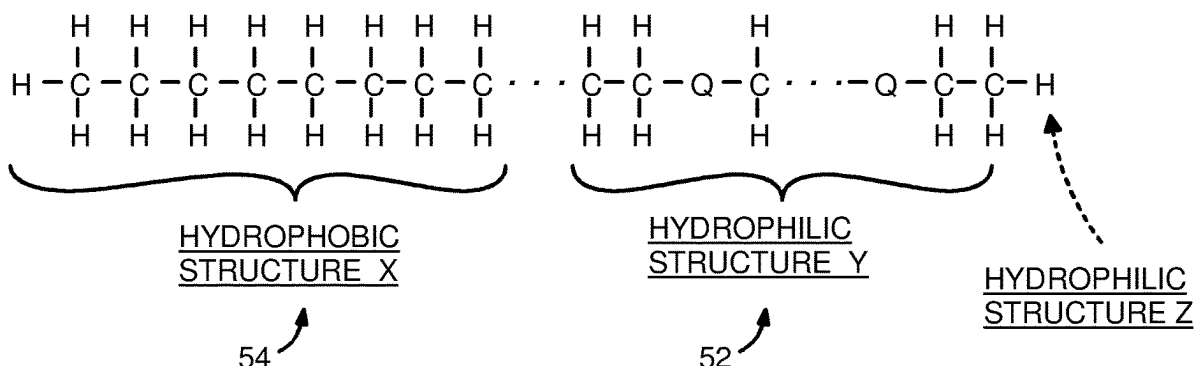
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Primary Examiner — Wojciech Haske
(74) *Attorney, Agent, or Firm* — Stuart T. Auvinen;
gPatent LLC

(57) **ABSTRACT**

Reagents A, B, C are added to an electrolyte bath for co-depositing tin-bismuth alloys (Sn—Bi). Reagent A is a larger acid molecule that binds to Bi^{3+} ions while reagent B is a small molecule that binds to the Bi^{3+} ions in spaces between the reagent A molecules. Reagents A and B reduce the standard electrode potential difference of Sn and Bi to permit co-deposition rates that yield a Sn—Bi alloy of 30-70% Bi by weight, around the 58% eutectic, with an alloy melting point below 180° C. for use as a low-temperature solder. Reagent C has a hydrophilic end that attaches to the electrode surface and a hydrophobic tail that is an aliphatic chain that attracts hydrogen gas, removing H_2 gas from the electrode surface. Reagent C improves alloy microstructure by removing H_2 gas generated at the cathode that can block Bi^{3+} ions from uniformly depositing on the surface.

13 Claims, 17 Drawing Sheets



(12)
United States Patent
Ng et al.

(10) **Patent No.:** **US 12,524,371 B2**
(45) **Date of Patent:** **Jan. 13, 2026**

- (54)
ENHANCED HARVARD ARCHITECTURE REDUCED INSTRUCTION SET COMPUTER (RISC) WITH DEBUG MODE ACCESS OF INSTRUCTION MEMORY WITHIN A UNIFIED MEMORY SPACE

(58)
Field of Classification Search
CPC G06F 11/00; G06F 11/22; G06F 11/26; G06F 11/3648; G06F 11/3656; G06F 9/30043; G06F 15/7817; G06F 13/4022
See application file for complete search history.
- (71)
Applicant: **High Tech Technology Limited**, Hong Kong (HK)

(72)
Inventors: **Chik Wai (David) Ng**, Hong Kong (HK); **Ka Lok (Roy) Ng**, Hong Kong (HK); **Yat Him (Hugo) Wong**, Hong Kong (HK); **Tze Fan Wong**, Hong Kong (HK); **King Yeung (Sunny) Chan**, Hong Kong (HK); **Ho Ming (Steve) Chim**, Hong Kong (HK); **Wai Kei (Timothy) Or**, Hong Kong (HK); **Chi Hong Chan**, Hong Kong (HK)

(73)
Assignee: **High Tech Technology Limited**, Hong Kong (HK)

(*)
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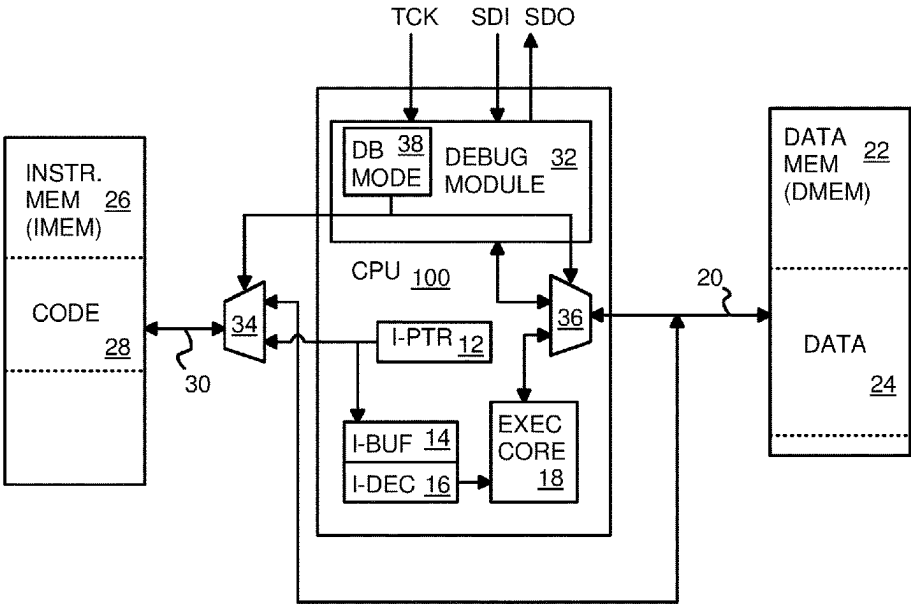
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Primary Examiner — David J. Huisman
Assistant Examiner — Emilio Alcantara-Ramos
(74) *Attorney, Agent, or Firm* — gPatent LLC; Stuart T. Auvinen

(57)
ABSTRACT
A Harvard-architecture computer simultaneously reads instructions using an instruction bus and accesses data over a separate data bus. A debug module has an external interface to an external debugger that initiates a debugging session by setting a debug bit in a debug mode register. When the debug bit is set, a first mux disconnects an instruction pointer and an instruction buffer from the instruction bus and instead connects the data bus to the instruction bus. A second mux disconnects a load/store unit in an execution core from the instruction bus and instead connects the debug module to the instruction bus. The external debugger sees a unified memory space and writes addresses to the debug module that are sent through the second mux to access the data memory, and instruction addresses are sent through the second mux and the first mux to the instruction memory to read or write instructions.

18 Claims, 8 Drawing Sheets
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The diagram illustrates a Harvard-architecture computer system (20) with a unified memory space. It includes an INSTR. MEM. 26 (IMEM) containing CODE 28. A CPU 100 is connected to the IMEM via a multiplexer 34 and a bus 30. The CPU 100 contains an I-PTR 12, an I-BUF 14, an I-DEC 16, and an EXEC CORE 18. A DEBUG MODULE 32 is connected to the CPU 100 and includes a DB MODE 38. The system also includes a DATA MEM. 22 (DMEM) containing DATA 24. A multiplexer 36 connects the CPU 100 to the DATA MEM. 22 via a bus 20. External interfaces TCK, SDI, and SDO are shown at the top.

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621 Patents Issued

After 32 years of writing patents as a full-time Patent Agent, 621 applications that I've written have now issued as patents. Congratulations inventors!

You can view the 621 issued patents I've written at:

www.gpatent.com

Rates Set for 2027

My hourly rate for 2027 will be \$510 per hour, billed in quarter-hour increments. Fixed-price quotes are available for patent applications to facilitate budgeting and avoid expensive surprises.

Prosecution work such as amendments and other paperwork is billed at the hourly rate. Litigation-support work is billed at a higher rate. Patent searches are billed at a flat \$800 for U.S. abstract searches. Patents can be viewed on-line.

Stuart T. Auvinen
429 26th Ave.
Santa Cruz, CA 95062

(831) 476-5506

Gpatent@Gmail.com
www.gpatent.com

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Stuart Auvinen is a Patent Agent registered with the U.S. Patent Office (Reg. No. 36,435). He is a former IC design engineer who writes patents for high-tech companies.

Stuart T. Auvinen

Patent Agent

429 26th Ave.
Santa Cruz, CA 95062-5319

Address Correction Requested